

#### **Feature**

- Precision MEMS process
- High performance, shielded, Micro-cavity structure
- Silicon substrate, 50Ω CPW output
- Au wire bonding, for MCM applications

## **Environmental Specifications**

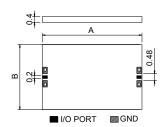
| Operating Temperature | -55℃~+85℃    |  |
|-----------------------|--------------|--|
| Storage Temperature   | -55°C∼+125°C |  |
| Max. Input Power      | 35dBm        |  |

# Electrical Specifications(T<sub>A</sub>=+25°C)

| Parameter                     | Min.  | Тур. | Max. | Unit |
|-------------------------------|---|------|------|------|
| Center Freq. (f₀)             | -   | 21.8 | -    | GHz  |
| Pass Band                     | 21.2  | -    | 22.4 | GHz  |
| Ripple in Pass band           | -   | -    | 1    | dB   |
| Insertion Loss @ f₀           | -   | -    | 3.5  | dB   |
| Return Loss                   | 12  | -    | -    | dB   |
|                               | ≥30@20.3GHz&23.2GHz                               |      |      | dB   |
| Out of band                   | ≥40@19.8GHz&23.3GHz                               |      |      | dB   |
| Attenuation                   | ≥55@DC~19GHz<br>≥50@24~32GHz<br>≤0.5@21.2~22.4GHz |      |      | dB   |
|                               |   |      |      | dB   |
| Group Delay Variation         |   |      |      | ns   |
| Linear Phase ≤±5@21.2~22.4GHz |   |      | Z    | 0    |

S2P file name: SiMS21R8\_1R2-8D3.s2p

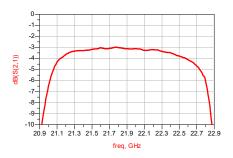
# **Outline Drawing**



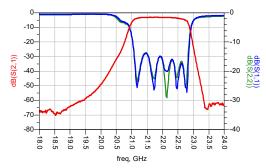
|  | Symbol | Value (mm) |         |      |
|--|--------|------------|---------|------|
|  |        | Min.       | Nominal | Max. |
|  | А      | 9.4        | -       | 9.5  |
|  | В      | 3.4        | -       | 3.5  |

### **Typical Test Curves**

Insertion Loss VS Frequency (T<sub>A</sub>=25°C)



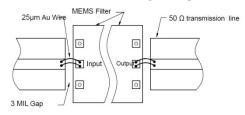
Insertion Loss & Return Loss VS Frequency (T<sub>A</sub>=25°C)



Broadband Insertion Loss VS Frequency (T<sub>A</sub>=25°C)

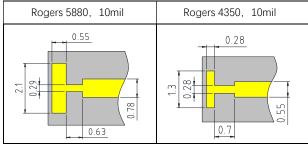


#### **Recommended Assembly Diagrams**



### **Application Notes:**

- 1. The chip is back-metalized and can be die mounted with AuSn eutectic performs or with electrically conductive epoxy (for example ME8456).
- 2. The die should be assembled on carriers like Kovar or Mu-Cu which have same Coefficient of thermal expansion. (2.9ppm/ $^{\circ}$ C) with Silicon, thickness 0.2mm max.
- 3. Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.
- 4. Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers.
- 5. Recommended to use T structure as below for bonding.



6. If you have any questions, please contact us.