

## Feature

- High Precision GaAs process
- High performance, shielded
- GaAs substrate, 50Ω CPW output
- Au wire bonding, for MCM applications

## Environmental Specifications

Operating Temperature	-55°C~+85°C
Storage Temperature	-65°C~+150°C
Max. Input Power	30dBm

## Electrical Specifications( $T_A=+25^\circ\text{C}$ )

Parameter	Min.	Typ.	Max.	Unit
Center Freq. ( $f_0$ )	-	1.23	-	GHz
Pass band	0.85	-	1.7	GHz
Insertion Loss @ $f_0$	-	-	1.5	dB
Ripple in Pass band	-	-	1.0	dB
Return Loss	12	-	-	dB
Out of band Attenuation	$\geq 30@0.55\text{GHz}$			dB
	$\geq 30@2.3\text{GHz}$			dB

S2P file name: PDBF-R7\_2-6C2.s2p

## Outline Drawing

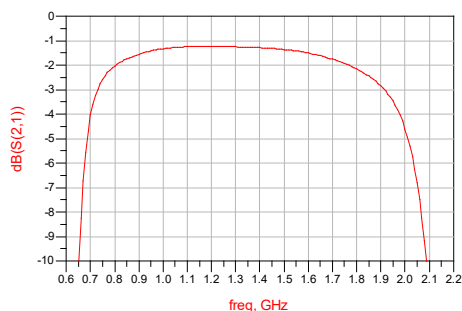


Notes:

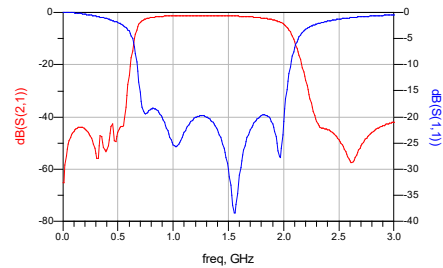
1. Dimensions are in millimeters. Tolerance:  $\pm 0.05\text{mm}$
2. Die thickness is 0.15 mm
3. Typical bond pad is  $0.1 \times 0.1 \text{ mm}^2$ .
4. The bottom of the device is gold plated, should be grounded.

## Typical Test Curves

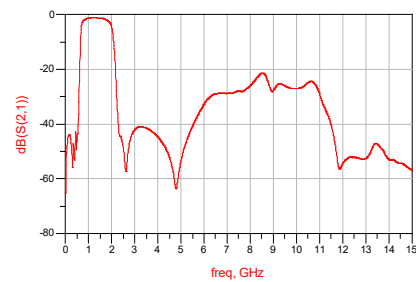
Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



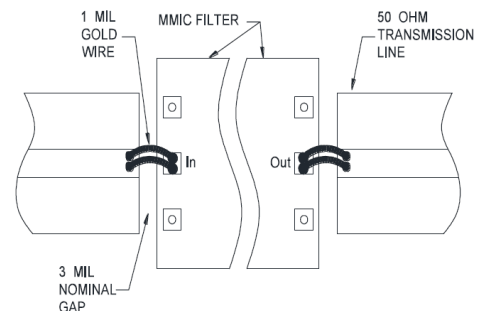
Insertion Loss & Return Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



Broadband Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



## Recommended Assembly Diagrams



## Application Notes:

1. The chip is back-metallized and can be die-mounted with AuSn eutectic preforms or with electrically conductive epoxy.
2. The die should be assembled on carriers like Kovar or Mu-Cu which have same Coefficient of thermal expansion. ( $5.8 \times 10^{-6}/^\circ\text{C}$ ) with GaAs.
3. Recommend using  $\Phi 25\mu\text{m}$  Au wire for bonding, whose length is around 400um.
4. Sinter by AuSn (80/20), which doesn't exceed  $300^\circ\text{C}$  within 30 seconds max.
4. Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.
5. Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers.
6. The device is sensitive to ESD. ESD protection is required during storage and usage.
7. If you have any questions, please contact us.