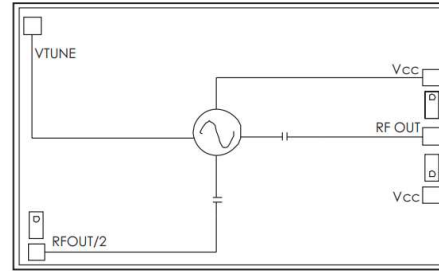


Performance

- Dual paths output: $F_0=9.5\sim 10.8\text{GHz}$
 $F_0/2=4.75\sim 5.4\text{GHz}$
- Output Power: +10dBm
- Noise figure: -109dBc/Hz @ 100KHz Typ
- Chip size: 2.5*1.6*0.1mm

Function Diagram

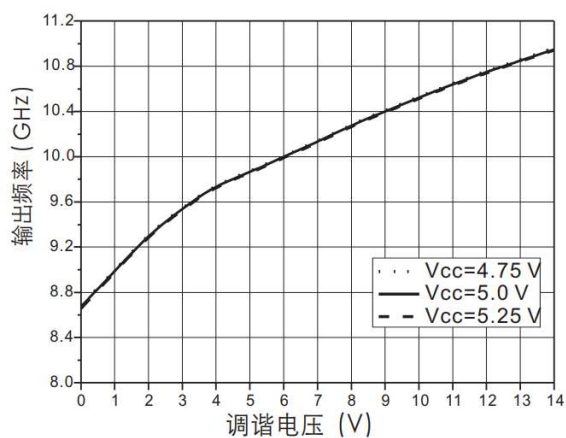


Electrical Specifications (Ta=+25°C, Vcc=+5V)

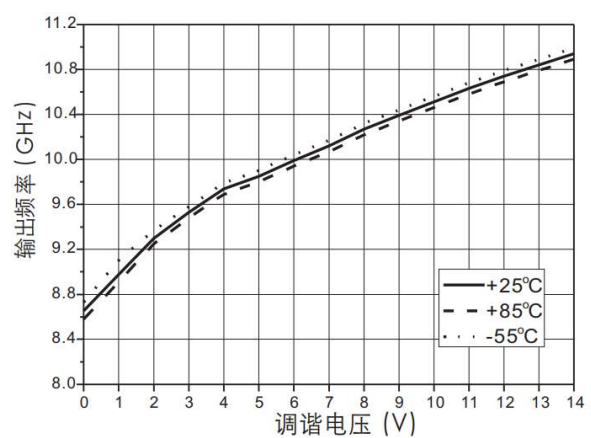
Parameter		Min	Typical	Max	Unit
Frequency Range	F0	9.5~10.8			GHz
	F0/2	4.75~5.4			GHz
Output Power	RFOUT	7	10	14	dBm
	RFOUT/2	6	9	13	dBm
Noise figure@100KHz, VTUNE=+5V@RFOUT		-	-109	-	dBc/Hz
Tuning Voltage		2	-	14	V
Harmonics	1/2	-	-30	-	dBc
	2 nd	-	-10	-	dBc
Frequency Pulling (12dB RL)		-	8	-	MHz
Pushing Frequency Factor @ VTUNE=5V		-	15	-	MHz/V
Frequency Shift		-	0.9	-	MHz/°C
Operating Current		150	190	230	mA

Test Curves (Die chip test)

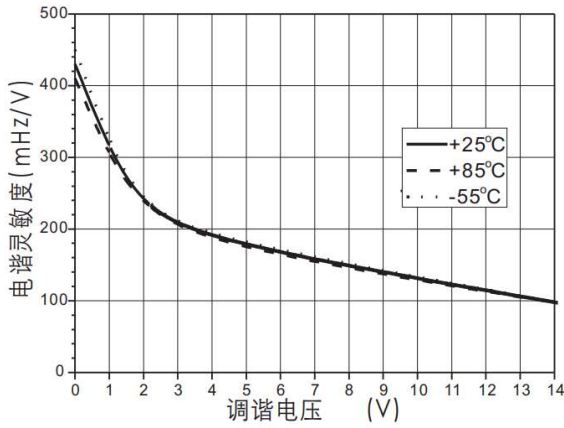
Output Freq vs. Tuning Voltage, TA=+25°C



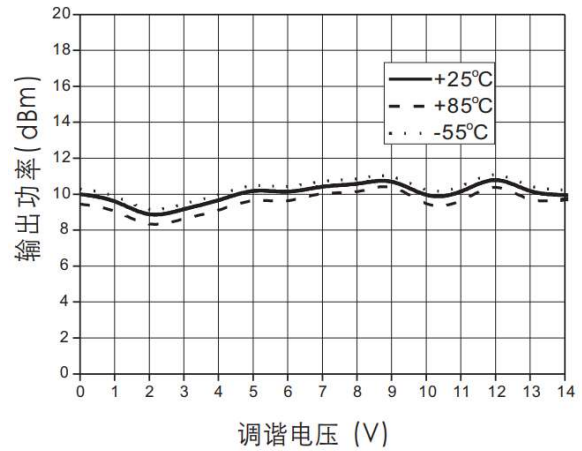
Output Freq vs. Tuning Voltage, Vcc=+5V



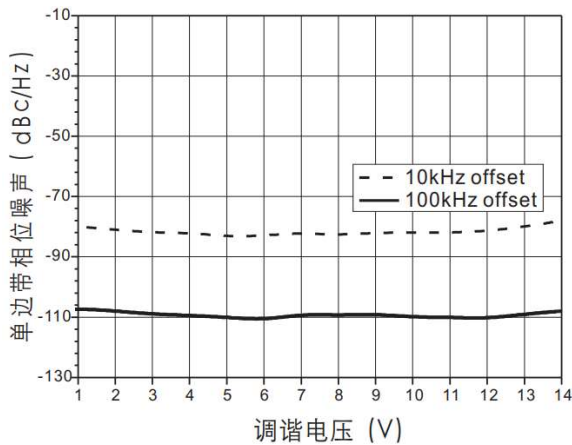
Electronic tuning sensitivity vs. Tuning Voltage
Vcc=+5V



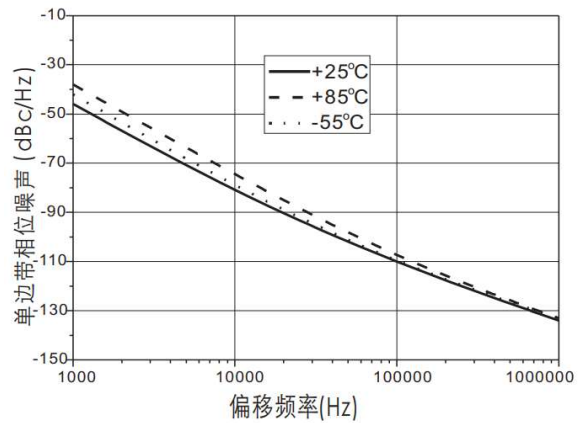
Output Power vs. Tuning Voltage, Vcc=+5V



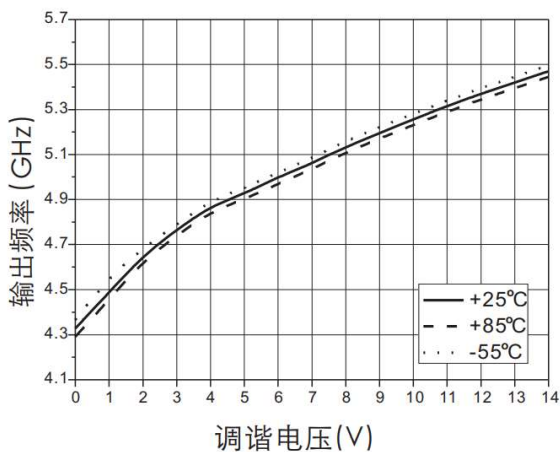
SSB Noise Figure vs. Tuning Voltage



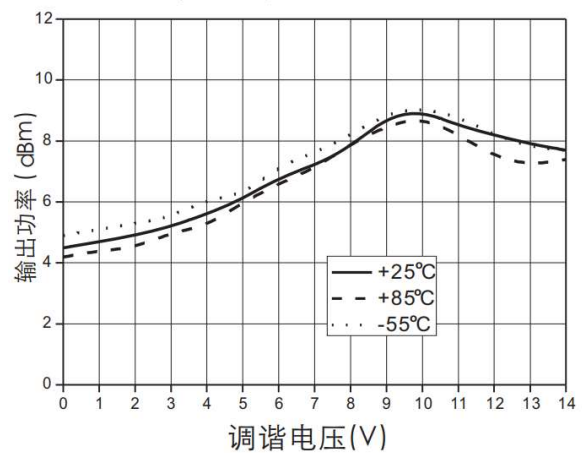
SSB Noise Figure vs. Vtune=+5V



RFOUT/2 Frequency vs. Tuning Voltage
Vcc=+5V



RFOUT/2 Output Power vs. Tuning Voltage
Vcc=+5V



Absolute Ratings

Vcc	+5.5Vdc
Vtune	0~+15V
Junction Temperature	175°C
Storage Temperature	-65°C~+150°C
Operating Temperature	-55°C~+125°C
Static Protection	Class 1A

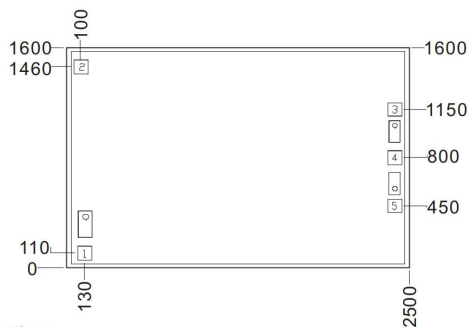
Typical Operating Current

Vcc(V)	ICC(mA)
4.75	185
5.0	210
5.25	235



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

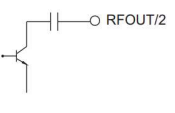
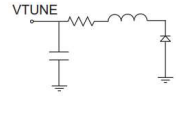
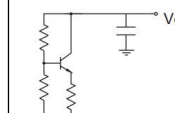
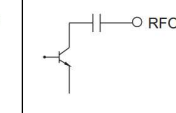
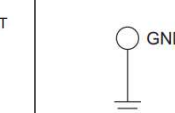
Outline Size



Note:

1. Unit: μm
2. Bottom side is gold plated
3. Bottom side is GND
4. Bonding pads is gold plated,
Pad size: $100 \times 100 (\mu\text{m})$
5. Don't bonding on thru holds
6. Tolerance: $\pm 50 \mu\text{m}$

Bonding Pads Definition

Number	1	2	3,5	4	
Symbol	RFOUT/2	VTUNE	Vcc	RF OUT	GND
Description	1/2 harmonic output (block capacitor included)	Tuning Voltage port	Current port, +5V	RF output port (block capacitor included)	Bottom must be grounded
Equivalent Circuit					

Assembly Drawing

