Feature

Pass Bands: 3GHz~4.8GHz, 4.3GHz~6.5GHz, 6GHz~8GHz, 7.5GHz~10GHz;

Insertion Loss in pass bands: ≤7.5dB

Isolation between pass bands: ≥30dB

Size: 3.6x3.3x0.1mm

Description

This device is a GaAs monolithic integrated FET switch filter bank chip. Adopt +5V/0V logic control; operating current is 25mA typ. and switching time is less than 30ns typ. It has low loss, excellent isolation, and high integration.

The metallization processing of thru-holes on the plate ensures good grounding. Extra grounding measures aren't required, which is easy for application. The back metallization is suitable for eutectic sintering or conductive adhesive sticking processes.

Absolute Rating

Control Voltage	-1.5V~+6V
Input Power	27dBm
Storage Temperature	-65~+150℃
Operating Temperature	-55~+125℃

Electrical Specifications 1 (T_A=+25℃)

Spec.	Pass band 1	Pass band 2	Unit
Freq. Range	3~4.8	4.3~6.5	GHz
Insertion Loss	≤6.5	≤7.0	dB
Rejection	≥20@1.9G&6.5G	≥20@2.7G&7.8G	dBc
	≥40@1.2G&8.5G	≥40@1.7G&8.8G	dBc
VSWR	≤2		

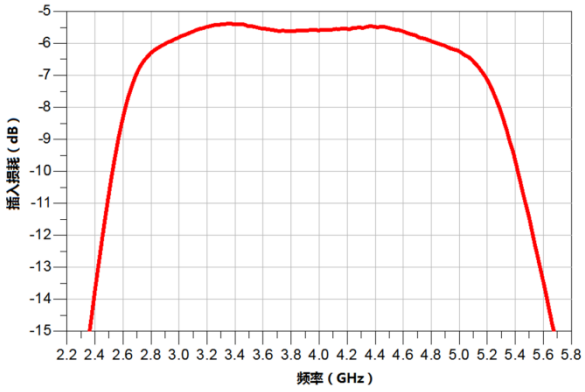
Electrical Specifications 2 (T_A=+25℃)

Spec.	Pass band 3	Pass band 4	Unit
Freq. Range	6~8	7.5~10	GHz
Insertion Loss	≤7.5	≤7.0	dB
Rejection	≥20@4.85G&10G	≥20@5.8G&13G	dBc
	≥40@4.4G&13.2G	≥40@5.2G&17.5G	dBc
VSWR	≤2		

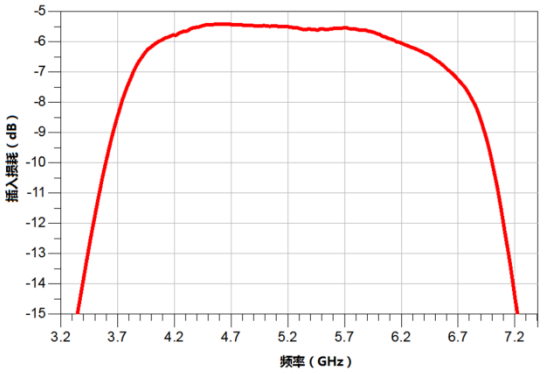
S2P file name: BWSBF-3_10-4.s2p

Typical Test Curves

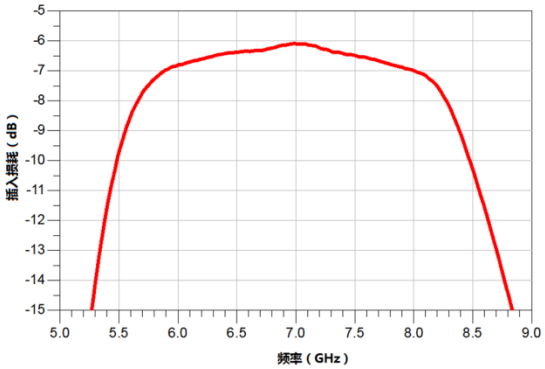
Pass band 1 Insertion Loss VS Frequency (T_A=25℃)



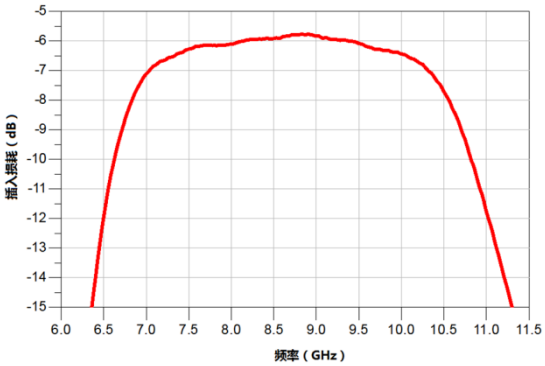
Pass band 2 Insertion Loss VS Frequency (T_A=25℃)



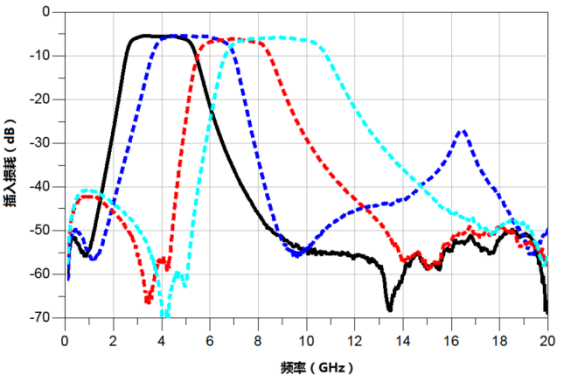
Pass band 3 Insertion Loss VS Frequency (T_A=25℃)



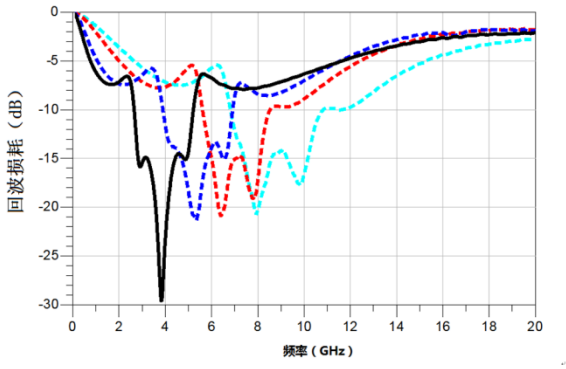
Pass band 4 Insertion Loss VS Frequency (T_A=25℃)



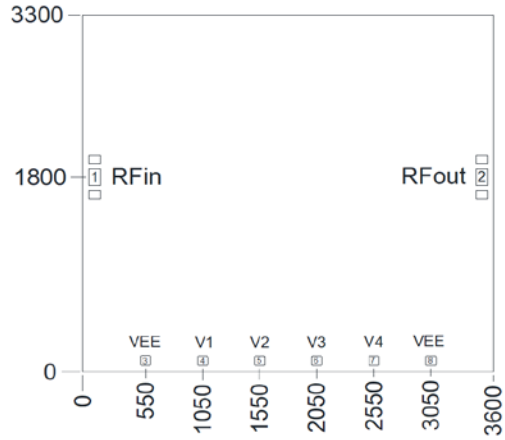
Insertion Loss VS Frequency (T_A=25℃)



Return Loss VS Frequency (T_A=25℃)



Mechanical Specification



Truth Table

Control Voltage (VEE=-5V)				Pass bands
V1	V2	V3	V4	
0	1	1	1	3GHz~4.8GHz
1	0	1	1	4.3GHz~6.5GHz
1	1	0	1	6GHz~8GHz
1	1	1	0	7.5GHz~1GHz
Status：Low（0）0V；High（1）+5V				

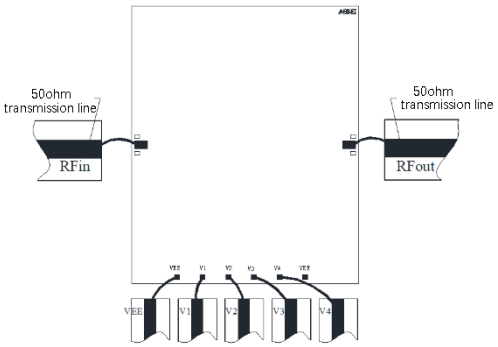
PINS Definitions

Pin No.	Symbol	Description
1,2	RFin， RFout	RF Input, RF Output
4,5,6,7	V1,V2,V3,V4	Control ports

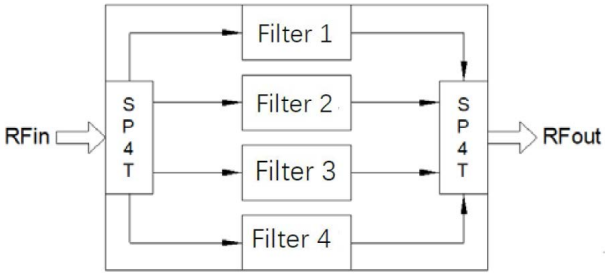
Notes:

1. Dimensions are um. Tolerance: ±0.05mm
2. Die thickness is 0.1mm
3. Typical bond pad is 100um *100um, which is 50um away from chip edge.
4. The bottom of the device is gold plated, should be grounded.

Recommended Assembly Diagrams



Functional Diagram



Application Notes:

1. The chip is back-metallized and can be die-mounted with AuSn eutectic preforms or with electrically conductive epoxy.
2. The die should be assembled on carriers like Kovar or Mu-Cu which have same Coefficient of thermal expansion. (5.8×10-6/) with GaAs.
3. Recommend using Φ25um Au wire for bonding, whose length is around 200um.
4. Sinter by AuSn (80/20), which doesn't exceed 300℃ within 30 seconds max.
4. Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.
5. Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers.
6. The device is sensitive to ESD. ESD protection is required during storage and usage.
7. If you have any questions, please contact us.