

## Feature

Pass Bands: 0.2GHz ~ 0.3GHz, 0.3GHz ~ 0.45GHz, 0.45GHz ~ 0.7GHz, 0.7GHz ~ 1.1GHz, 1.1GHz ~ 1.8GHz, 1.8GHz ~ 3GHz;

Insertion Loss in pass bands:  $\leq 9$ dB

Isolation between pass bands:  $\geq 30$ dB

Size: 5x6x0.15mm

## Description

This device is a FET switch filter bank MMIC based on GaAs processing. Adopt +5V/0V logic control, switching time is less than 30ns typ. It has low loss, excellent isolation, and high integration.

The metallization processing of thru-holes on the plate ensures good grounding. Extra grounding measures aren't required, which is easy for application. The back metallization is suitable for eutectic sintering or conductive adhesive sticking processes.

## Absolute Rating

Control Voltage	-1V~+5V
Input Power	27dBm
Storage Temperature	-65~+150°C
Operating Temperature	-55~+125°C

## Electrical Specifications 1 (T<sub>A</sub>=+25°C)

Spec.	Pass band 1	Pass band 2	Unit
Freq. Range	0.2~0.3	0.3~0.45	GHz
Insertion Loss	$\leq 8$	$\leq 8$	dB
Rejection	$\geq 35@0.07\text{GHz}\&0.45\text{GHz}$	$\geq 35@0.12\text{GHz}\&0.65\text{GHz}$	dBc
VSWR	$\leq 2$		—

## Electrical Specifications 2 (T<sub>A</sub>=+25°C)

Spec.	Pass band 3	Pass band 4	Unit
Freq. Range	0.45~0.7	0.7~1.1	GHz
Insertion Loss	$\leq 9$	$\leq 9$	dB
Rejection	$\geq 35@0.15\text{GHz}\&1\text{GHz}$	$\geq 35@0.3\text{GHz}\&1.5\text{GHz}$	dBc
VSWR	$\leq 2$		—

## Electrical Specifications 3 (T<sub>A</sub>=+25°C)

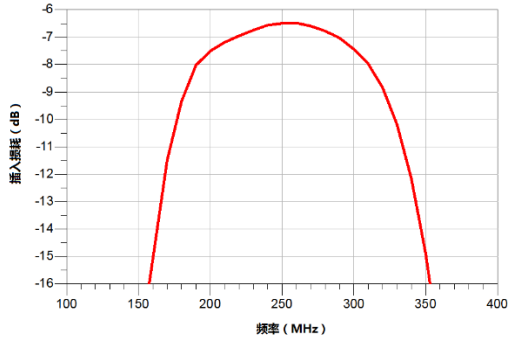
Spec.	Pass band 5	Pass band 6	Unit
Freq. Range	1.1~1.8	1.8~3	GHz
Insertion Loss	$\leq 9$	$\leq 8.5$	dB
Rejection	$\geq 35@0.4\text{GHz}\&2.3\text{GHz}$	$\geq 35@0.65\text{GHz}\&3.7\text{GHz}$	dBc

VSWR	$\leq 2$	—
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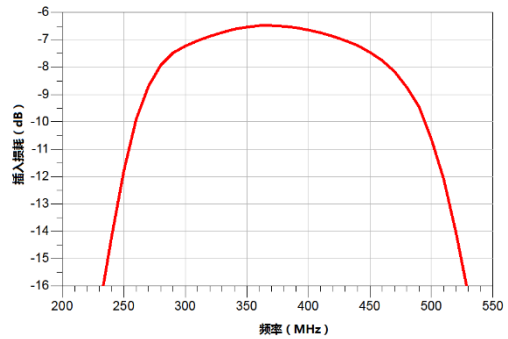
S2P file name: PDSBF-R2\_3-6.s2p

### Typical Test Curves

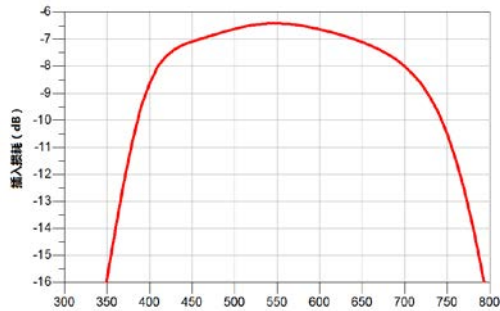
Pass band 1 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



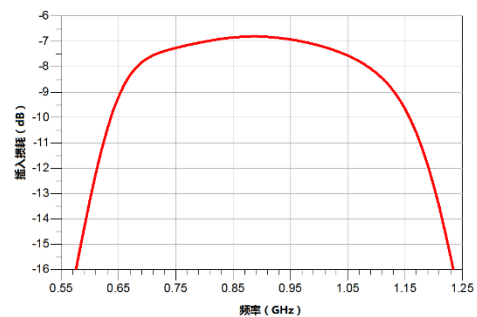
Pass band 2 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



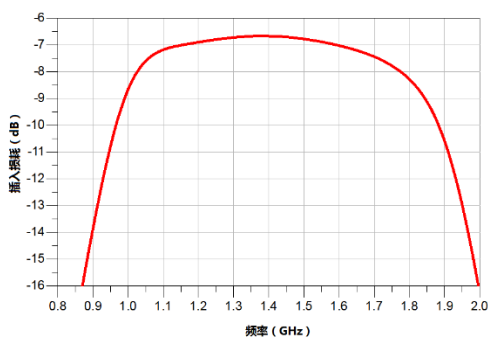
Pass band 3 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



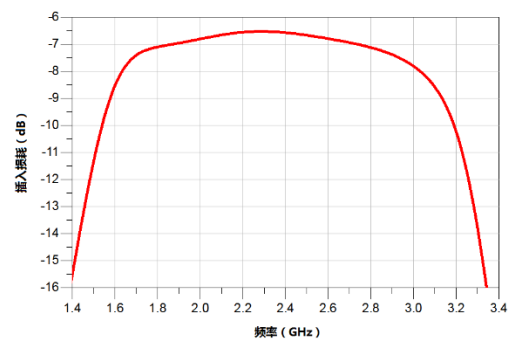
Pass band 4 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



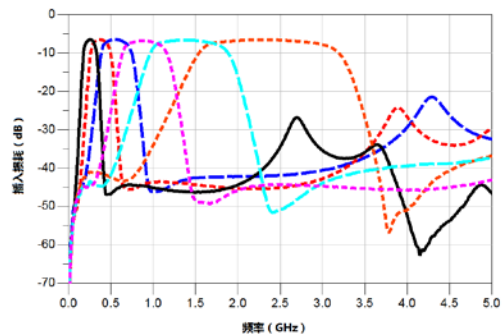
Pass band 5 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



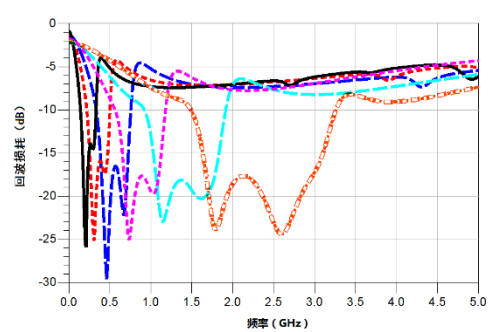
Pass band 6 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



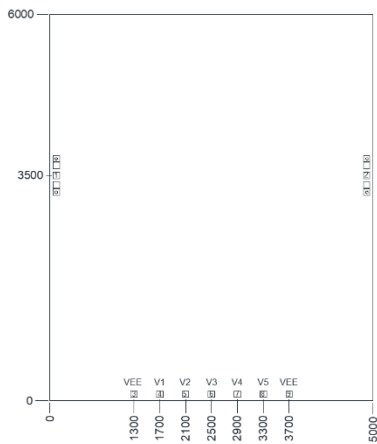
Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



Return Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



## Mechanical Specification



## Truth Table

Control Voltage (VEE=-5V)					Pass bands
V1	V2	V3	V4	V5	
0	1	0	0	1	0.2GHz~0.3GHz
1	0	0	1	0	0.3GHz~0.45GHz
0	1	1	0	0	0.45GHz~0.7GHz
1	0	0	0	1	0.7GHz~1.1GHz
0	1	0	1	0	1.1GHz~1.8GHz
1	0	1	0	0	1.8GHz~3GHz

Status: Low (0) 0V; High (1) +5V

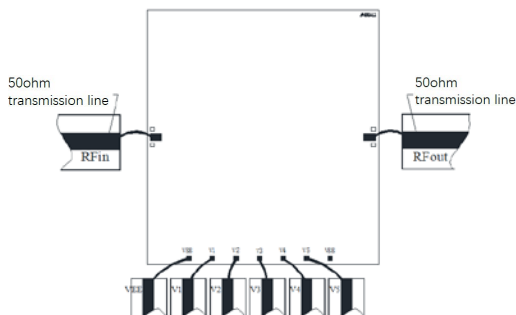
## PINS Definitions

Pin No.	Symbol	Description
1,2	RFin, RFout	RF Input, RF Output
4,5,6,7,8	V1,V2,V3,V4,V5	Control Ports
3,9	VEE	Driver Power Supply Voltage

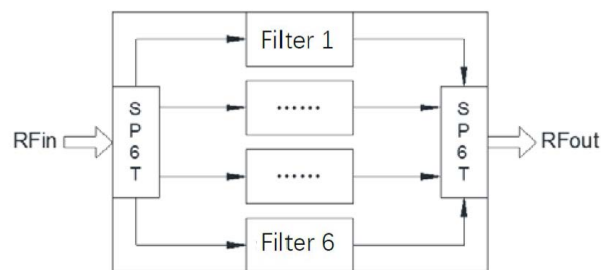
Notes:

1. Dimensions are  $\mu\text{m}$ . Tolerance:  $\pm 0.05\text{mm}$
2. Die thickness is 0.1mm
3. Typical bond pad is  $100\mu\text{m} \times 100\mu\text{m}$ , which is  $50\mu\text{m}$  away from chip edge.
4. The bottom of the device is gold plated, should be grounded.

## Recommended Assembly Diagrams



## Functional Diagram



## Application Notes:

1. The chip is back-metallized and can be die-mounted with AuSn eutectic preforms or with electrically conductive epoxy.
2. The die should be assembled on carriers like Kovar or Mu-Cu which have same Coefficient of thermal expansion. ( $5.8 \times 10^{-6}/^\circ\text{C}$ ) with GaAs.
3. Recommend using  $\Phi 25\mu\text{m}$  Au wire for bonding, whose length is around 200 $\mu\text{m}$ .
4. Sinter by AuSn (80/20), which doesn't exceed  $300^\circ\text{C}$  within 30 seconds max.
4. Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.
5. Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers.
6. The device is sensitive to ESD. ESD protection is required during storage and usage.
7. If you have any questions, please contact us.