

## Feature

Pass Bands: 7.8GHz ~ 9.1GHz, 8.2GHz ~ 9.8GHz, 8.8GHz ~ 10.9GHz;

This chip can be combined with BWSBF-9R9/14R2-3、BWSBF-13R2/18R5-4、BWSBF-17R5/31R1-3、BWSBF-30R1/40-2 to cover frequency 8-40GHz.

Insertion Loss in pass bands:  $\leq 4.6$ dB

Isolation between pass bands:  $\geq 30$ dB

Size: 4.0x4.3x0.1mm

## Description

This chip is a monolithic integrated PIN switch filter. Adopt +5V/-5V logic control, operating current 25mA typ. and switching time is less than 20ns typ. It has low loss, excellent isolation, and high integration.

The metallization processing of thru-holes on the plate ensures good grounding. Extra grounding measures aren't required, which is easy for application. The back metallization is suitable for eutectic sintering or conductive adhesive sticking processes.

## Absolute Rating

Control Voltage	-1.5V~+6V
Input Power	30dBm
Storage Temperature	-65~+150°C
Operating Temperature	-55~+125°C

## Electrical Specifications 1 ( $T_A = +25^\circ\text{C}$ )

Spec.	Pass band 1	Pass band 2	Unit
Freq. Range	7.8~9.1	8.2~9.8	GHz
Insertion Loss	$\leq 4.6$	$\leq 4.4$	dB
Rejection	$\geq 20$ @6.9GHz&10.16GHz	$\geq 20$ @7.27GHz&10.2GHz	dBc
	$\geq 40$ @6.6GHz&11.2GHz	$\geq 40$ @6.9GHz&12.13GHz	dBc
VSWR	$\leq 1.8$		—

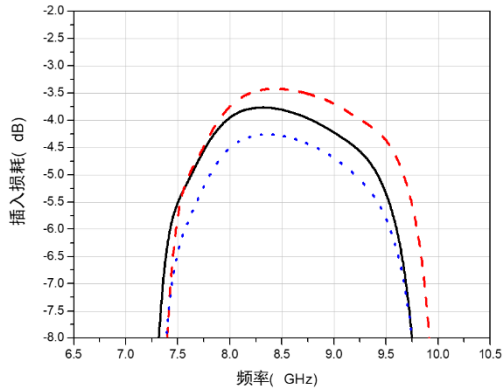
## Electrical Specifications 2 ( $T_A = +25^\circ\text{C}$ )

Spec.	Pass band 3	Unit
Freq. Range	8.8~10.9	GHz
Insertion Loss	$\leq 4.2$	dB
Rejection	$\geq 20$ @7.8GHz&12.4GHz	dBc
	$\geq 40$ @7.35GHz&12.9GHz	dBc
VSWR	$\leq 1.8$	—

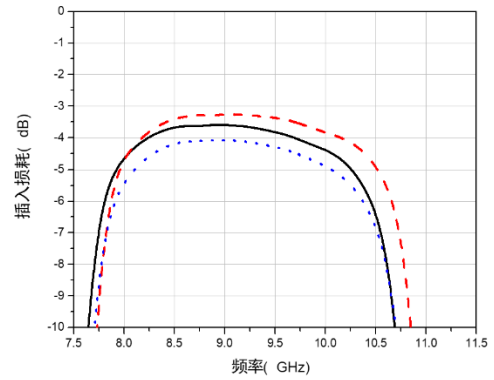
S2P file name: BWSBF-7R8\_10R9-3.s2p

## Typical Test Curves

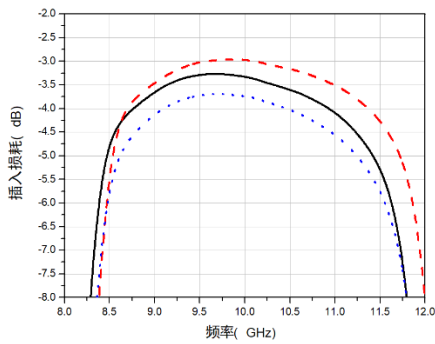
Pass band 1 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



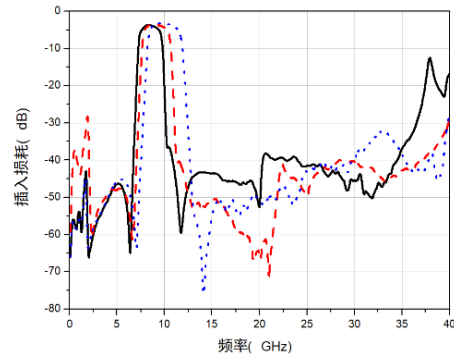
Pass band 2 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



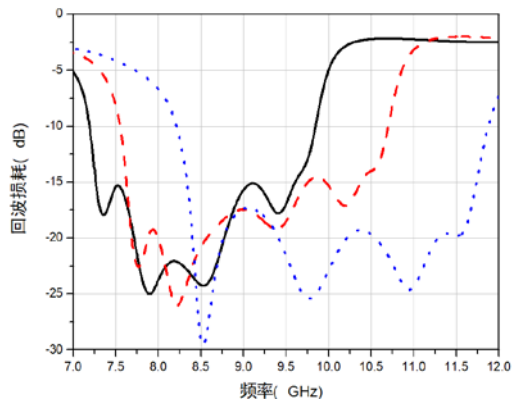
Pass band 3 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



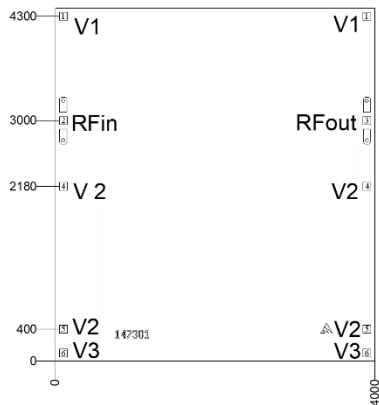
Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



Return Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



### Mechanical Specification



### Truth Table

Control Voltage			Pass bands
V1	V2	V3	
0	1	1	7.8GHz~9.1GHz
1	0	1	8.2GHz~9.8GHz
1	1	0	8.8GHz~10.9GHz
Status: Low (0) -5V; High (1) +5V			

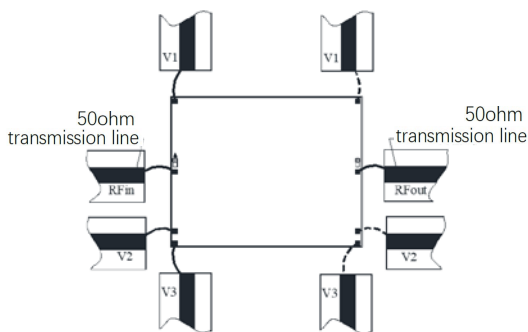
### PINS Definitions

Pin No.	Symbol	Description
2, 3	RFin, RFout	RF Input, RF Output
1, 4, 5, 6	V1, V2, V3	Control ports

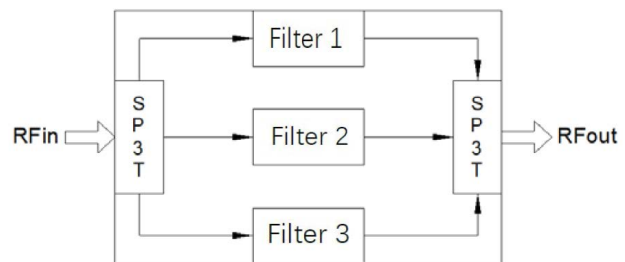
Notes:

1. Dimensions are um. Tolerance:  $\pm 0.05\text{mm}$
2. Die thickness is 0.1mm
3. Typical bond pad is 100um \*100um, which is 50um away from chip edge.
4. The bottom of the device is gold plated, should be grounded.

### Recommended Assembly Diagrams



### Functional Diagram



### Application Notes:

1. The chip is back-metallized and can be die-mounted with AuSn eutectic preforms or with electrically conductive epoxy.
2. The die should be assembled on carriers like Kovar or Mu-Cu which have same Coefficient of thermal expansion. ( $5.8 \times 10^{-6}/^\circ\text{C}$ ) with GaAs.
3. Recommend using  $\Phi 25\mu\text{m}$  Au wire for bonding, whose length is around 200um.
4. Sinter by AuSn (80/20), which doesn't exceed  $300^\circ\text{C}$  within 30 seconds max.
4. Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.
5. Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers.
6. The device is sensitive to ESD. ESD protection is required during storage and usage.
7. If you have any questions, please contact us.