

## Feature

Pass Bands: 9.85GHz ~ 10.9GHz, 10.6GHz ~ 11.65GHz, 11.35GHz ~ 12.4GHz, 12.1GHz ~ 12.15GHz;

Insertion Loss in pass bands:  $\leq 9$ dB

Isolation between pass bands:  $\geq 30$ dB

Size: 5.5x4.5x0.15mm

## Description

This device is a FET switch filter bank MMIC based on GaAs processing. Adopt +5V/0V logic control or -5V/0V logic control, switching time is less than 30ns typ. It has low loss, excellent isolation, and high integration.

The metallization processing of thru-holes on the plate ensures good grounding. Extra grounding measures aren't required, which is easy for application. The back metallization is suitable for eutectic sintering or conductive adhesive sticking processes.

## Absolute Rating

Control Voltage	-1V~+5V
Input Power	27dBm
Storage Temperature	-65~+150°C
Operating Temperature	-55~+125°C

## Electrical Specifications 1 ( $T_A = +25^\circ\text{C}$ )

Spec.	Pass band 1	Pass band 2	Unit
Freq. Range	9.85~10.9	10.6~11.65	GHz
Insertion Loss	$\leq 9$	$\leq 9$	dB
Rejection	$\geq 40@8.6\text{GHz}$	$\geq 40@9.3\text{GHz}$	dBc
	$\geq 40@12.5\text{GHz}$	$\geq 40@13.3\text{GHz}$	dBc
VSWR	$\leq 1.8$		—

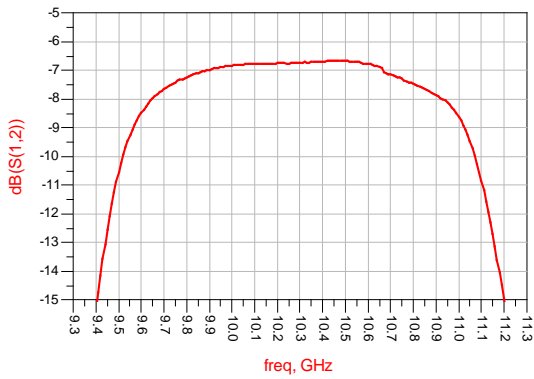
## Electrical Specifications 2 ( $T_A = +25^\circ\text{C}$ )

Spec.	Pass band 3	Pass band 4	Unit
Freq. Range	11.35~12.4	12.1~13.15	GHz
Insertion Loss	$\leq 9$	$\leq 9$	dB
Rejection	$\geq 40@10\text{GHz}$	$\geq 40@10.8\text{GHz}$	dBc
	$\geq 40@14\text{GHz}$	$\geq 40@14.5\text{GHz}$	dBc
VSWR	$\leq 1.8$		—

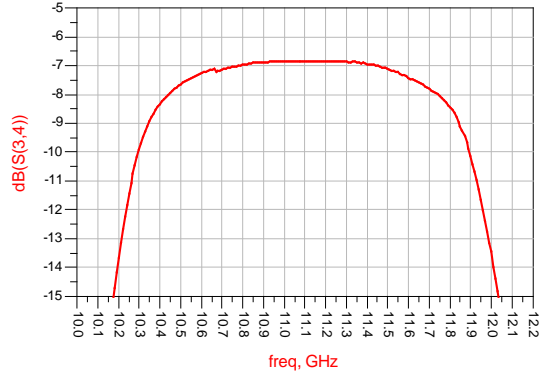
S2P file name: PDSBF4-9R85\_13R15-5D7.s2p

### Typical Test Curves

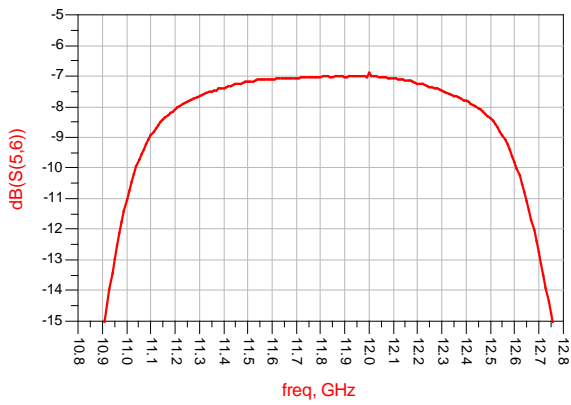
Pass band 1 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



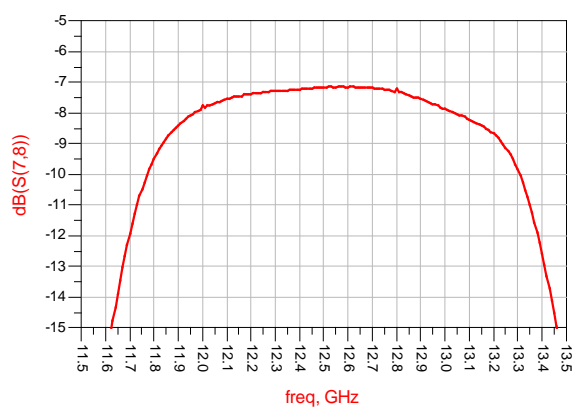
Pass band 2 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



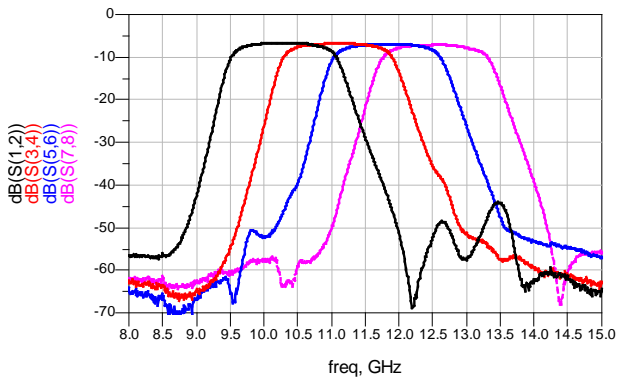
Pass band 3 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



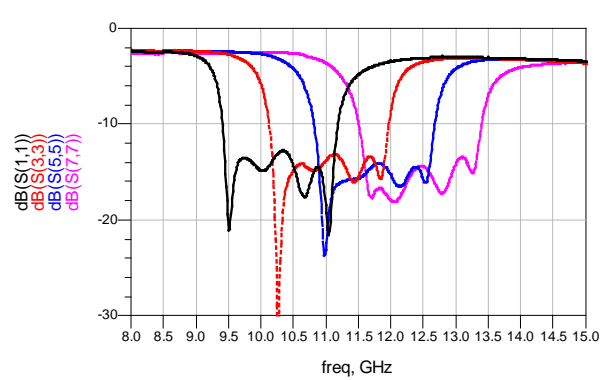
Pass band 4 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



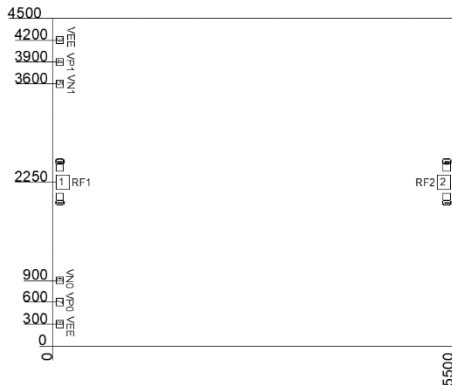
Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



Return Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



## Mechanical Specification



## Truth Table

Driver Voltage (VEE=-5V)				Pass bands
+5/0V Control		0/-5V Control		
VP1	VP0	VN1	VN0	
0V	0V	VN1	VN0	9.85-10.9GHz
0V	5V	-5V	-5V	10.6-11.65GHz
5V	0V	-5V	0V	11.35-12.4GHz
5V	5V	0V	-5V	12.1-13.15GHz

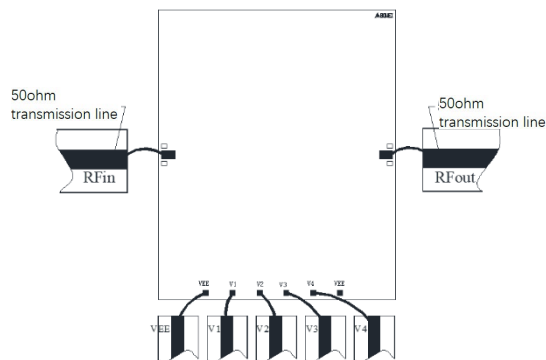
## PINS Definitions

Pin No.	Symbol	Description
1, 2	RF1, RF2	RF Input, RF Output
3, 8	VEE	Driver Power Supply Voltage
4, 7	VP1, VP0	+5/0V Control ports
5, 6	VN1, VN0	0/-5V Control ports

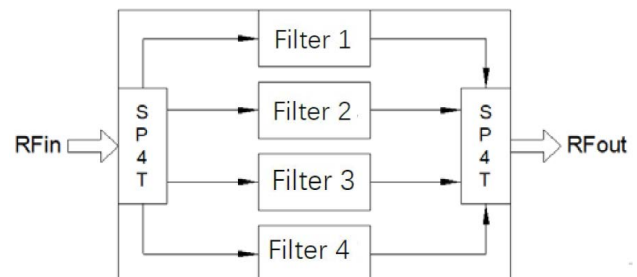
### Notes:

1. Dimensions are um. Tolerance:  $\pm 0.05\text{mm}$
2. Die thickness is 0.1mm
3. Typical bond pad is  $100\mu\text{m} \times 100\mu\text{m}$ , which is  $50\mu\text{m}$  away from chip edge.
4. The bottom of the device is gold plated, should be grounded.

## Recommended Assembly Diagrams



## Functional Diagram



## Application Notes:

1. The chip is back-metallized and can be die-mounted with AuSn eutectic preforms or with electrically conductive epoxy.
2. The die should be assembled on carriers like Kovar or Mu-Cu which have same Coefficient of thermal expansion. ( $5.8 \times 10^{-6}/^\circ\text{C}$ ) with GaAs.
3. Recommend using  $\Phi 25\mu\text{m}$  Au wire for bonding, whose length is around  $200\mu\text{m}$ .
4. Sinter by AuSn (80/20), which doesn't exceed  $300^\circ\text{C}$  within 30 seconds max.
4. Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.
5. Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers.
6. The device is sensitive to ESD. ESD protection is required during storage and usage.
7. If you have any questions, please contact us.