

## Feature

Pass Bands: 5.0GHz ~ 5.5GHz, 5.45GHz ~ 6.05GHz, 6.0GHz ~ 6.65GHz, 6.6GHz ~ 7.35GHz;

Insertion Loss in pass bands:  $\leq 10.5$ dB

Isolation between pass bands:  $\geq 30$ dB

Size: 4.5x4.5x0.15mm

## Description

This device is a FET switch filter bank MMIC based on GaAs processing. Adopt +5V/0V logic control, switching time is less than 30ns typ. It has low loss, excellent isolation, and high integration.

The metallization processing of thru-holes on the plate ensures good grounding. Extra grounding measures aren't required, which is easy for application. The back metallization is suitable for eutectic sintering or conductive adhesive sticking processes.

## Absolute Rating

Control Voltage	-1V~+5V
Input Power	27dBm
Storage Temperature	-65~+150°C
Operating Temperature	-55~+125°C

## Electrical Specifications 1 ( $T_A = +25^\circ\text{C}$ )

Spec.	Pass band 1	Pass band 2	Unit
Freq. Range	5.0~5.5	5.45~6.05	GHz
Insertion Loss	$\leq 10.5$	$\leq 10.5$	dB
Rejection	$\geq 30@4.4\text{GHz}$	$\geq 30@4.8\text{GHz}$	dBc
	$\geq 30@6.1\text{GHz}$	$\geq 30@6.6\text{GHz}$	dBc
VSWR	$\leq 1.8$		—

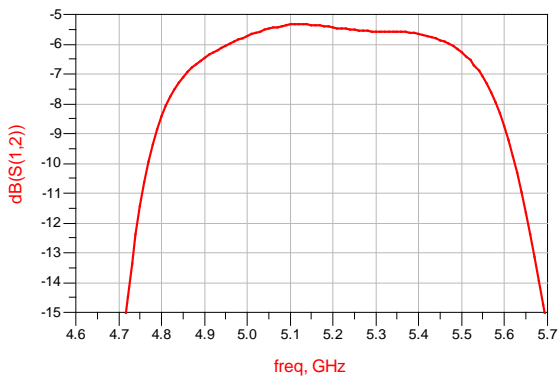
## Electrical Specifications 2 ( $T_A = +25^\circ\text{C}$ )

Spec.	Pass band 3	Pass band 4	Unit
Freq. Range	6.0~6.65	6.6~7.35	GHz
Insertion Loss	$\leq 10.5$	$\leq 10.5$	dB
Rejection	$\geq 30@5.2\text{GHz}$	$\geq 30@5.7\text{GHz}$	dBc
	$\geq 30@7.4\text{GHz}$	$\geq 30@8.1\text{GHz}$	dBc
VSWR	$\leq 1.8$		—

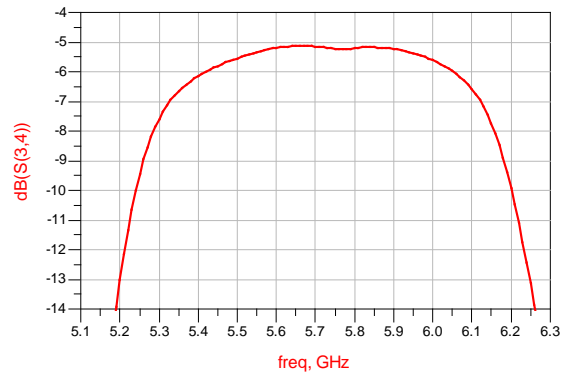
S2P file name: PDSBF4-5R05\_7R35-5D8.s2p

## Typical Test Curves

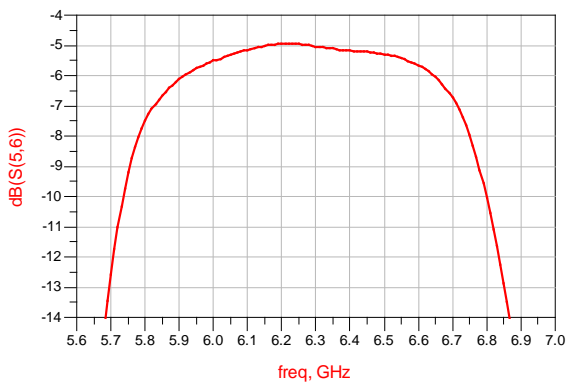
Pass band 1 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



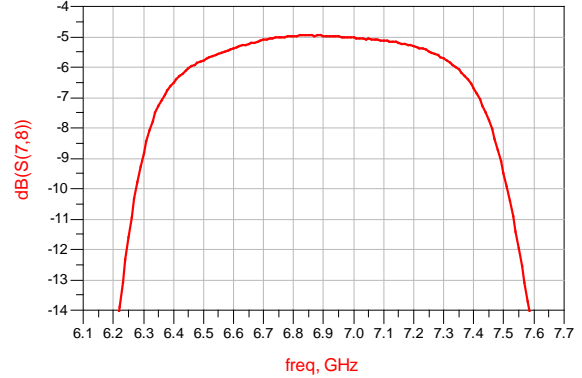
Pass band 2 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



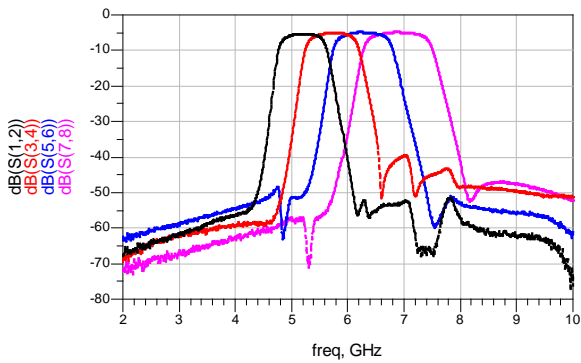
Pass band 3 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



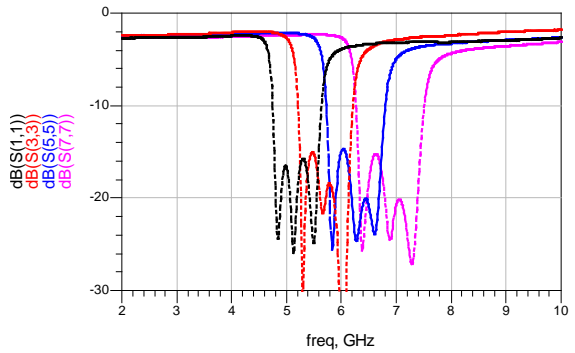
Pass band 4 Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



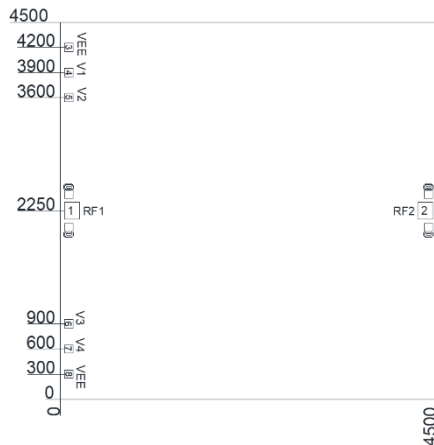
Insertion Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



Return Loss VS Frequency ( $T_A=25^\circ\text{C}$ )



## Mechanical Specification



## Truth Table

Driver Voltage (VEE = -5V)				Pass bands
V1	V2	V3	V4	
0V	5V	5V	5V	Pass band 1
5V	0V	5V	5V	Pass band 2
5V	5V	0V	5V	Pass band 3
5V	5V	5V	0V	Pass band 4

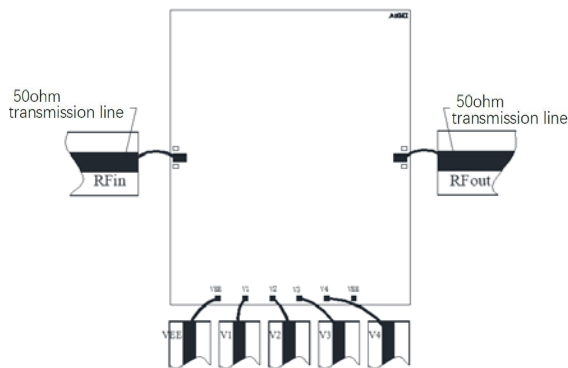
## PINS Definitions

Pin No.	Symbol	Description
1, 2	RF1, RF2	RF Input, RF Output
3, 8	VEE	Driver Power Supply Voltage
4, 5, 6, 7	V1, V2, V3, V4	Control ports

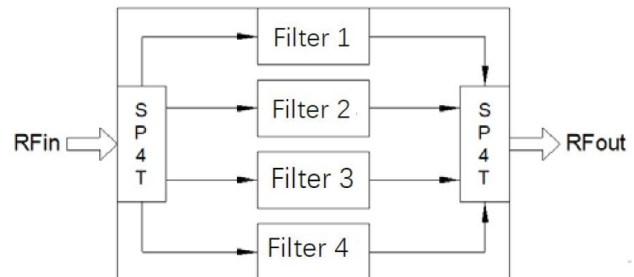
Notes:

1. Dimensions are um. Tolerance:  $\pm 0.05\text{mm}$
2. Die thickness is 0.1mm
3. Typical bond pad is  $100\text{um} \times 100\text{um}$ , which is  $50\text{um}$  away from chip edge.
4. The bottom of the device is gold plated, should be grounded.

## Recommended Assembly Diagrams



## Functional Diagram



## Application Notes:

1. The chip is back-metallized and can be die-mounted with AuSn eutectic preforms or with electrically conductive epoxy.
2. The die should be assembled on carriers like Kovar or Mu-Cu which have same Coefficient of thermal expansion. ( $5.8 \times 10^{-6}/^\circ\text{C}$ ) with GaAs.
3. Recommend using  $\Phi 25\text{um}$  Au wire for bonding, whose length is around  $200\text{um}$ .
4. Sinter by AuSn (80/20), which doesn't exceed  $300^\circ\text{C}$  within 30 seconds max.
4. Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.
5. Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers.
6. The device is sensitive to ESD. ESD protection is required during storage and usage.
7. If you have any questions, please contact us.