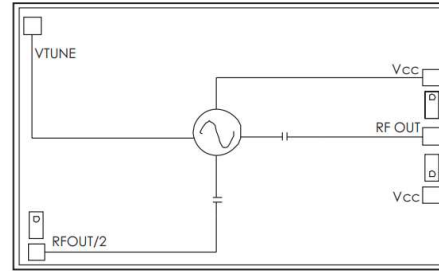


Performance

- Dual paths output: $F_0=11.0\sim 12.4\text{GHz}$
 $F_0/2=5.5\sim 6.2\text{GHz}$
- Output Power: +10dBm
- Noise figure: -108dBc/Hz @ 100KHz Typ
- Chip size: 2.5*1.6*0.1mm

Function Diagram

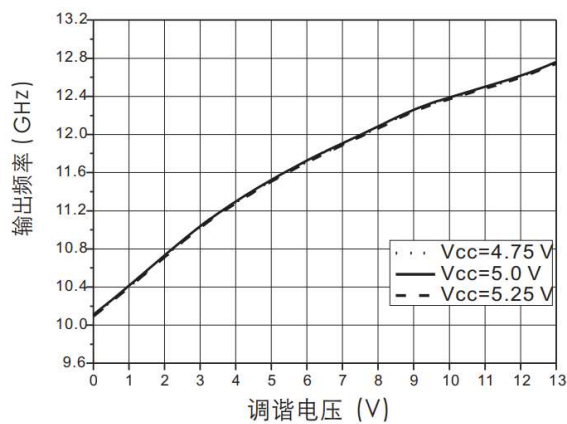


Electrical Specifications (Ta=+25°C, Vcc=+5V)

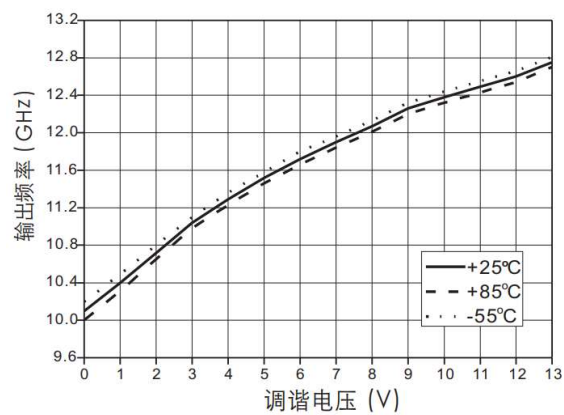
Parameter		Min	Typical	Max	Unit
Frequency Range	F0	11.0~12.4			GHz
	F0/2	5.5~6.2			GHz
Output Power	RFOUT	6	10	14	dBm
	RFOUT/2	8	11	14	dBm
Noise figure@100KHz, VTUNE=+5V@RFOUT		-	-108	-	dBc/Hz
Tuning Voltage		2	-	13	V
Harmonics	1/2	-	-20	-	dBc
	2 nd	-	-20	-	dBc
Frequency Pulling (12dB RL)		-	10	-	MHz
Pushing Frequency Factor @ VTUNE=5V		-	20	-	MHz/V
Frequency Shift		-	1.1	-	MHz/°C
Operating Current		160	200	250	mA

Test Curves (Die chip test)

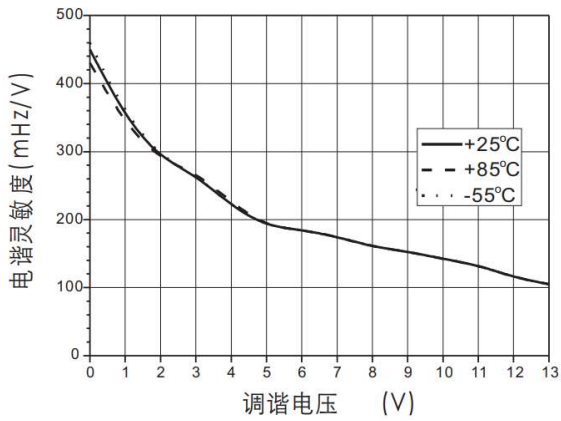
Output Freq vs. Tuning Voltage, TA=+25°C



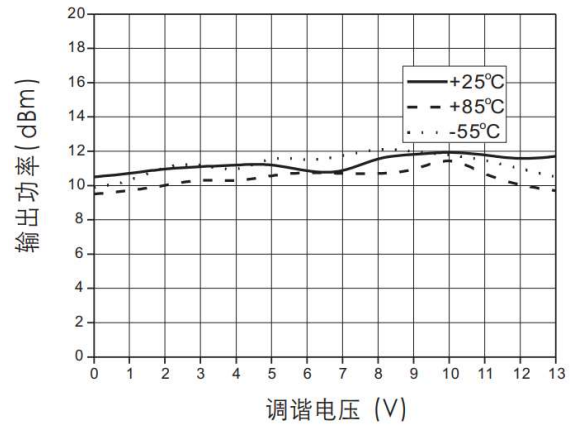
Output Freq vs. Tuning Voltage, Vcc=+5V



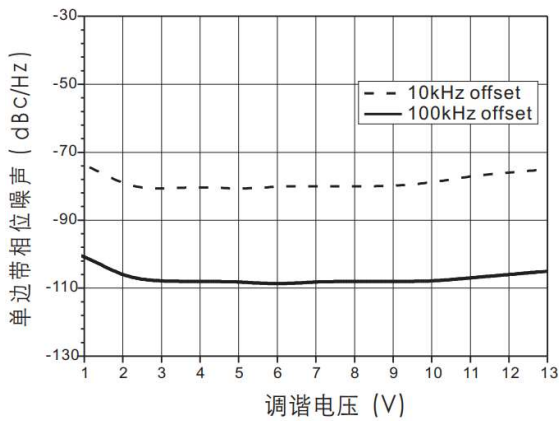
Electronic tuning sensitivity vs. Tuning Voltage
Vcc=+5V



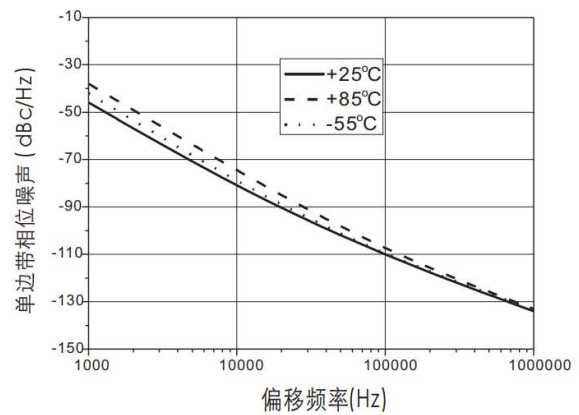
Output Power vs. Tuning Voltage, Vcc=+5V



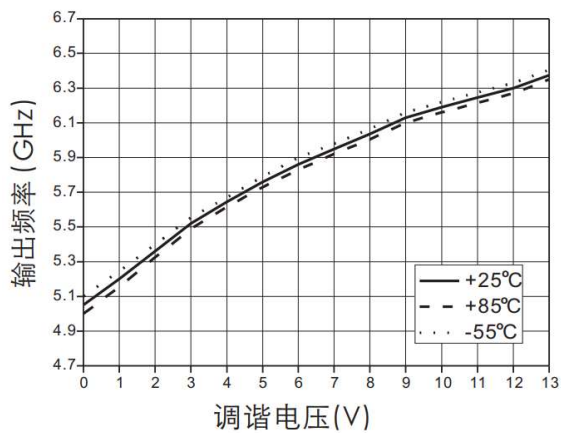
SSB Noise Figure vs. Tuning Voltage



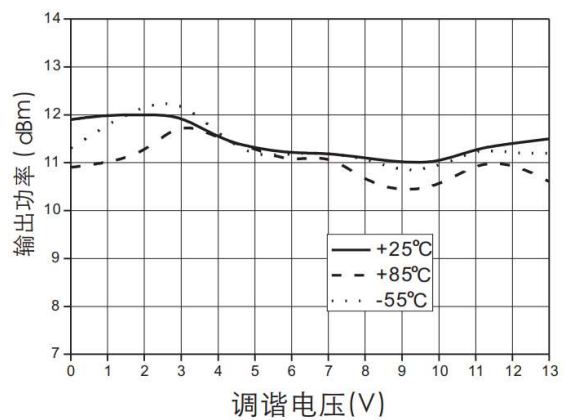
SSB Noise Figure vs. Vtune=+5V



RFOUT/2 Frequency vs. Tuning Voltage
Vcc=+5V



RFOUT/2 Output Power vs. Tuning Voltage
Vcc=+5V



Absolute Ratings

Vcc	+5.5Vdc
Vtune	0~+15V
Junction Temperature	175°C
Storage Temperature	-65°C~+150°C
Operating Temperature	-55°C~+125°C
Static Protection	Class 1A

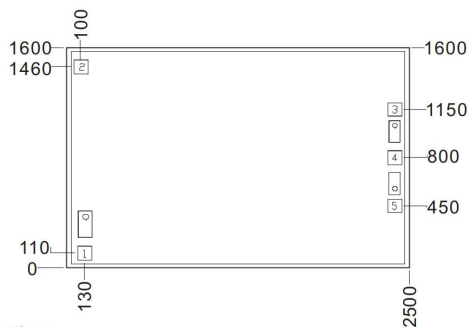
Typical Operating Current

Vcc(V)	ICC(mA)
4.75	175
5.0	200
5.25	225



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

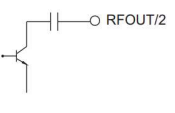
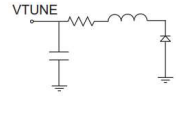
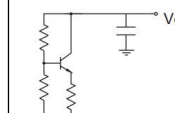
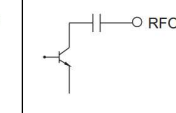
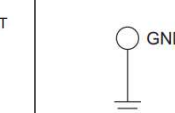
Outline Size



Note:

1. Unit: um
2. Bottom side is gold plated
3. Bottom side is GND
4. Bonding pads is gold plated,
Pad size: 100*100(um)
5. Don't bonding on thru holds
6. Tolerance: ±50um

Bonding Pads Definition

Number	1	2	3,5	4	
Symbol	RFOUT/2	VTUNE	Vcc	RF OUT	GND
Description	1/2 harmonic output (block capacitor included)	Tuning Voltage port	Current port, +5V	RF output port (block capacitor included)	Bottom must be grounded
Equivalent Circuit					

Assembly Drawing

