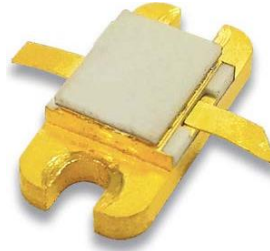


Performance

- Technology: 0.5um Power GaN HEMT
- Frequency: 0.138~0.138GHz
- Typical Pout: 40dBm(CW)
- Typical Gain: 17dB
- Typical PAE: 65%
- Bias: 30V/-2.8V
- Package: Metal Ceramic



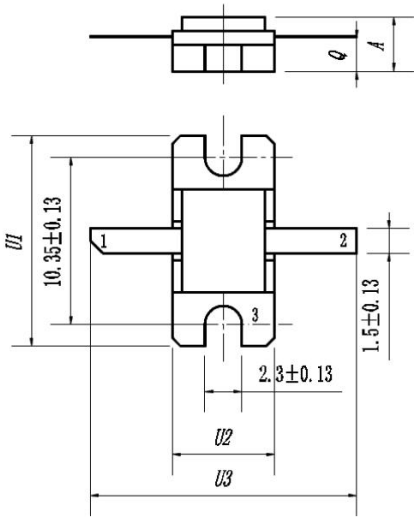
Electrical Specifications (T_A=25°C, V_d=30V(CW), V_g=-2.8V, F: 0.138~0.138GHz)

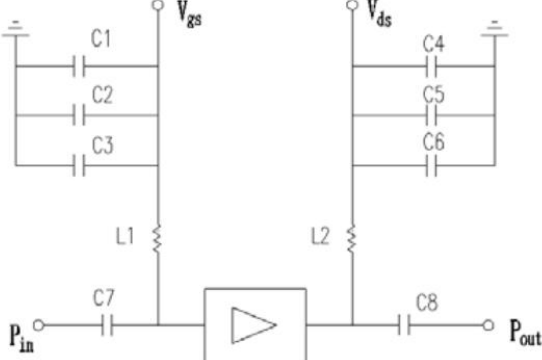
Symbol	Parameter	Min	Typical	Max	Unit
Pout	Output Power	-	40	-	dBm
Gp	Power Gain	-	17	-	dB
η _{add}	Power Added Efficiency	-	65	-	%

Absolute Max Ratings (T_A=25°C)

Symbol	Parameter	Value	Remark
V _d	Drain Voltage	50V	
V _g	Grid Voltage	-5V	
T _{ch}	Channel Temperature	225°C	【1】
T _m	Mounting Temperature	300°C	1 min, N ₂ Protection
T _{stg}	Storage Temperature	-55~125°C	
T _c	Operating Temperature	-55~85°C	

【1】 Exceeding any one or combination of these limits may cause permanent damage.

Outline Drawing	Dimension symbols																											
 The drawing shows a top view and a side view of the transistor. The top view is a square package with a central pad (1) and four side pads (2, 3, 4, 5). Dimensions include: total width 10.35±0.13, total height 1.5±0.13, central pad width 2.3±0.13, and pad spacing U2 and U3. The side view shows a height A and a diameter Q.	<table><tr><th rowspan="2">Symbol</th><th colspan="3">Value (unit: mm)</th></tr><tr><th>Min.</th><th>Typ.</th><th>Max.</th></tr><tr><td>A</td><td>-</td><td>3.38</td><td>3.80</td></tr><tr><td>U1</td><td>12.80</td><td>13.00</td><td>13.20</td></tr><tr><td>U2</td><td>6.15</td><td>6.35</td><td>6.55</td></tr><tr><td>U3</td><td>16.26</td><td>16.5</td><td>16.76</td></tr><tr><td>Q</td><td>1.90</td><td>2.07</td><td>2.24</td></tr></table>	Symbol	Value (unit: mm)			Min.	Typ.	Max.	A	-	3.38	3.80	U1	12.80	13.00	13.20	U2	6.15	6.35	6.55	U3	16.26	16.5	16.76	Q	1.90	2.07	2.24
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Application Circuit													
 The circuit diagram shows a GaN transistor with gate voltage V_{gs} and drain voltage V_{ds}. The input P_{in} is connected to the gate through a series capacitor C7 and a parallel combination of capacitors C1, C2, and C3. The gate is also connected to ground through a parallel combination of capacitors C4, C5, and C6. The output P_{out} is connected to the drain through a series capacitor C8 and a parallel combination of capacitors C1, C2, and C3. Inductors L1 and L2 are connected between the gate and drain nodes.	<table> <tr> <th>No</th><th>Value</th></tr> <tr> <td>L1、L2</td><td>100nH</td></tr> <tr> <td>C1、C4</td><td>100pF</td></tr> <tr> <td>C2、C5</td><td>1000pF</td></tr> <tr> <td>C3、C6</td><td>>10uF(electrolytic capacitor or tantalum capacitor)</td></tr> <tr> <td>C7、C8</td><td>620pF</td></tr> </table>	No	Value	L1、L2	100nH	C1、C4	100pF	C2、C5	1000pF	C3、C6	>10uF(electrolytic capacitor or tantalum capacitor)	C7、C8	620pF
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C7、C8	620pF												

Note:

- (1) This product is a pre-matched tube, and the input and output impedance values are 50 ohms;
- (2) The power-on sequence shall be in strict accordance with the sequence of applying negative power first and then positive power. When power-off, the leakage voltage shall be reduced first and then the grid voltage shall be reduced;
- (3) This product is a high-power device. Pay attention to heat dissipation during use. The higher the shell temperature is, the shorter the service life is. The service temperature should not be higher than 80 °C;
- (4) This product is an electrostatic sensitive device. It needs to pay attention to electrostatic protection during storage and use, and it needs to be grounded well during use.