

Performance

- Technology: 0.35um Power GaN HEMT
- Frequency: 2.3~2.7GHz
- Typical Pout : 52dBm
- Typical Gain: 12dB
- Typical PAE: 55%
- Bias: 28V/-3V
- Package: Metal Ceramic

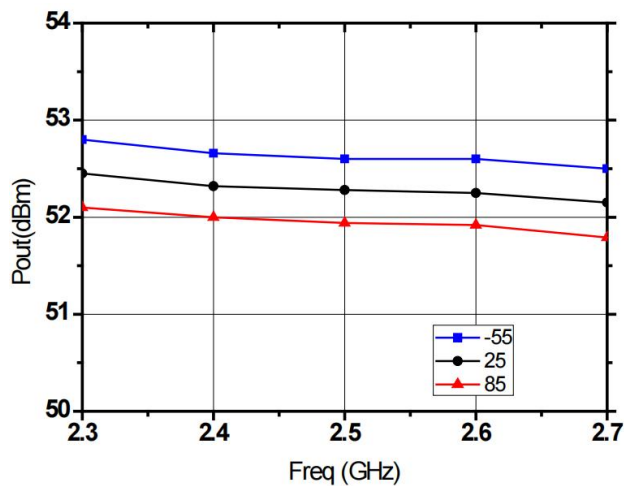


Electrical Specifications ($T_A=25^{\circ}\text{C}$, $V_d=28\text{V}$, $V_g=-3\text{V}$, $F: 2.3\sim 2.7\text{GHz}$, $PL=300\mu\text{s}$, $D.C=20\%$)

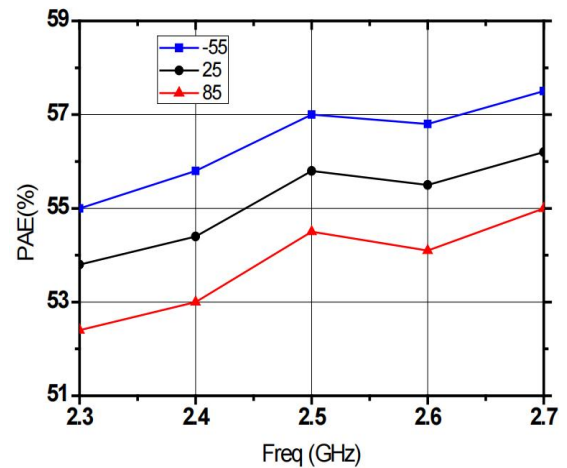
Symbol	Parameter	Min	Typical	Max	Unit
Pout	Output Power	51.5	52	-	dBm
G	Small Signal Gain	-	15	-	dB
Gp	Power Gain	-	12	-	dB
η_{add}	Power Added Efficiency	52	55	-	%
Rth	Thermal Resistance	-	-	0.55	$^{\circ}\text{C}/\text{W}$

Test Curves

Pout&Freq. @ Different Temp.



PAE&Freq. @ Different Temp.



Absolute Max Ratings (T_A=25°C)

Symbol	Parameter	Value	Remark
V _d	Drain Voltage	36V	
V _g	Grid Voltage	-5V	
T _{ch}	Channel Temperature	225°C	【1】
T _m	Mounting Temperature	300°C	1 min, N ₂ Protection
T _{stg}	Storage Temperature	-55~175°C	
T _c	Operating Temperature	-55~85°C	

【1】 Exceeding any one or combination of these limits may cause permanent damage.

Outline Drawing	Dimension Symbol														
The drawing consists of two views: a top view and a side view. The top view shows a central square pad with rounded corners, surrounded by a larger square frame with four semi-circular protrusions on each side. Dimensions include: overall width $U1$, overall height $U2$, distance between side protrusions 8 ± 0.25, distance between top protrusions $2 \times 0.6 \pm 0.05$, distance between bottom protrusions $2 \times 2.6 \pm 0.13$, and a central pad width of 20.4 ± 0.25. The side view shows the profile of the device with a total height A and a top layer thickness of 0.1 ± 0.03. Other side view dimensions include 1.4 ± 0.13 and 2.4 ± 0.25. A section line A-A is indicated.	<table><tr><th rowspan="2">Symbol</th><th colspan="2">Value (unit: mm)</th></tr><tr><th>Min.</th><th>Max.</th></tr><tr><td>U1</td><td>23.80</td><td>24.20</td></tr><tr><td>U2</td><td>17.20</td><td>17.60</td></tr><tr><td>A</td><td>-</td><td>5.2</td></tr></table>	Symbol	Value (unit: mm)		Min.	Max.	U1	23.80	24.20	U2	17.20	17.60	A	-	5.2
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U1	23.80	24.20													
U2	17.20	17.60													
A	-	5.2													

Application Circuit

The diagram shows a GaN Transistor (FET) circuit. The input is connected to a Port Pin through a capacitor C8. The input matching network consists of capacitors C1, C2, and C3. The gate is biased by a DC voltage source -Vg through a resistor R1. The gate is also connected to a microstrip line TL1. The drain is connected to a microstrip line TL2, which is then connected to a resistor R2 and a capacitor C4. The output is connected to a Port Pin through a capacitor C9. The circuit is powered by a DC voltage source -Vg.

Parameter	Symbol	Value	Unit
Filter capacitor	C1,C2,C4, C5,C6	1000	pF
Filter capacitor	C3,C7	100	pF
DC isolation capacitance	C8,C9	20	pF
Stabilizing resistance	R1	15	Ω
Resistance	R2	50	Ω
Microstrip line	TL1,TL2	$\lambda/4$	-

Note:

- (1) This product is an internal matching tube, with input and output impedance values of 50 ohms;
- (2) The power-on sequence shall be in strict accordance with the sequence of applying negative power first and then positive power. When power-off, the leakage voltage shall be reduced first and then the grid voltage shall be reduced;
- (3) This product is a high-power device. Pay attention to heat dissipation during use. The higher the shell temperature is, the shorter the service life is. The service temperature should not be higher than 80 °C;
- (4) This product is an electrostatic sensitive device. It needs to pay attention to electrostatic protection during storage and use, and it needs to be grounded well during use.